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10/761,204	01/22/2004	Noriaki Oda	8017-1122	2345

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EXAMINER	
WILLIAMS, ALEXANDER O	

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2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/761,204	ODA	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 to 11, 14 and 42 to 49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 to 11, 14 and 42 to 49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/761204 Attorney's Docket #: 8017-1122
Filing Date: 1/22/2004; claimed foreign priority to 1/30/2003

Applicant: Oda Examiner: Alexander Williams

Applicant's election of the species of figure 2 (claims 1 to 11, 14 and 42 to 49), filed 8/30/05, has been acknowledged.

Claims 12, 13 and 15 to 41 have been cancelled.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The use of the trademark on page 10, line 24 has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

The disclosure is objected to because of the following informalities: On page 9, lines 7, "and upper copper layer 100" and line13, "Lower copper layer 100" are both labeled the same. It appear that the –Lower copper layer" should be labeled "200".

Appropriate correction is required.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 11, 14 and 42 to 49, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(b) as being anticipated by Saran (U.S. Patent # 6,232,662 B1).

1. Saran (figures 1 to 6) specifically figure 2 show a semiconductor device, comprising: bonding pads **241** that are formed on a semiconductor substrate **200**; an upper copper layer **230** that is formed on the lower surface of said bonding pads with a barrier metal interposed; and a lower copper layer **210** that is formed closer to said semiconductor substrate than said upper copper layer; wherein a copper area of said lower copper layer under said bonding pads is equal to or lower than that of said upper copper layer.

2. A semiconductor device according to claim 1, Saran show wherein said lower copper layer is electrically insulated from said upper copper layer.

3. A semiconductor device according to claim 1, Saran show wherein the copper area ratio of said upper copper layer is greater than that of other copper layers that are formed as circuit interconnects on said semiconductor substrate.

4. A semiconductor device according to claim 1, Saran show wherein the copper area ratio of said upper copper layer is at least 70%.

5. A semiconductor device according to claim 1, Saran show wherein the planar dimensions of said bonding pads and said upper copper layer are substantially equal.

6. A semiconductor device according to claim 1, Saran show wherein said upper copper layer is constituted by a plurality of copper layers.

7. A semiconductor device according to claim 6, Saran show wherein the copper area ratios of each copper layer of said upper copper layer are substantially the same.

8. A semiconductor device according to claim 6, Saran further comprising: interlevel dielectric films that are provided between each of the copper layers of said upper copper layer; and via-plugs composed of copper that are embedded in said interlevel dielectric films wherein each of the copper layers of said upper copper layer are connected by way of said via-plugs.

9. A semiconductor device according to claim 8, Saran show wherein the copper layer pattern of the copper layer that is positioned uppermost in said upper copper layer and said via--plugs that are connected to the copper layer pattern are embedded in a dielectric film that is composed of a first material.

10. A semiconductor device according to claim 1, Saran show wherein the copper area ratio of said lower copper layer is at least 15% and not greater than 95%.

11. A semiconductor device according to claim 1, Saran show wherein said lower copper layer is constituted by a plurality of copper layers.

14. A semiconductor device according to claim 13, Saran show wherein each of the copper layers of said lower copper layer are constituted by a copper pattern that is embedded in a dielectric

film that is composed of a second material having a lower relative dielectric constant than said first material.

42. Saran (figures 1 to 6) specifically figure 2 show a semiconductor device comprising: a bonding region in which a bonding pad **241** is formed; an internal circuit region provided inside of said bonding region, said internal circuit region having a multilevel wiring structure that includes a plurality of copper interconnect layers **210,220** at a first level and a plurality of copper interconnect layers **220,230** at second level; and

a copper layer formed in said bonding region under said bonding pad in electrical contact therewith, one of said copper interconnect layers at said first level being elongated from said internal circuit region to said bonding region under said copper layer in electrical isolation therefrom.

43. The device as claimed in claim 42, Saran show wherein one of said copper interconnect layers at said second level is further elongated from said internal circuit region to said bonding region under said copper layer in electrical isolation from said copper layer and from one of said copper interconnect layers at said first level.

44. The device as claimed in claim 42, Saran show wherein said copper layer includes first and second copper layers and a via-plug sandwiched therebetween.

45. The device as claimed in claim 44, Saran show wherein said multilevel wiring structure further includes a plurality of copper interconnect layers at a third level and a plurality

of copper interconnect layers at a fourth level, said first copper layer being formed at said third level and said second copper layer being formed at said fourth level.

46. The device as claimed in claim 45, Saran show wherein said bonding pad is in electrical contact with said second copper layer, and one of said copper interconnect layers at said fourth level has an electrical contact with said second copper layer.

(23) Dielectric layer 304, about 200 to 1000 nm thick, comprises any good quality dielectric such as plasma oxide. It may also consist of FSG, USG, PSG oxides, or some polymeric such as polyimide. Layers 305 and 306, about 20 to 50 nm thick, are made of nitride or oxynitride. Dielectric layer 307, about 200 to 1000 nm thick, comprises material with low dielectric constant, such as HSQ, or a stack of oxide (FSG, USG, PSG oxides) and HSQ.

(24) Crucial for the present invention are metal patterns 31 and 32. They are, for instance, circuit interconnects made of copper, with dense layout rules. Widths 31a and 32a can vary from about 0.15 to 50 .mu.m, and spacing 33a is in the 0.1 to 1.0 range. Patterns 31 and 32 may be surrounded by thin barrier layers 308 similar to layer 301. Metal patterns 31 and 32 may exhibit vias 31b and 32b, about 0.1 to 0.5 nm wide, which reach through pre-metal dielectric layer 309 (typically USG or PSG oxides) to various lower levels in order to make electrical connections to other active or passive circuit elements located under the bond pad area. In FIG. 3, via 31b connects to poly-silicon layer 310 (about 100 to 300 nm thick and surrounded by sidewall spacer oxide or nitride 311), and via 32b connects to silicide layer 312. This silicide layer terminates in trench isolation 313, which may be 50 to 300 nm wide and extend 200 to 500 nm deep into silicon substrate 314. The gate width 310a of the MOS transistor is often in the 0.1 to 0.5 .mu.m range, while the overall transistor width is typically 0.5 to 1.0 .mu.m.

(25) Referring now to FIG. 4, the hierarchy of layers, their material compositions and geometries are analogous to those in

FIG. 3. In contrast to FIG. 3, though, the embodiment of FIG. 4 does not comprise the dense circuit pattern of metal interconnects (reference numerals 31 and 32) under bond pad 40. It requires, therefore, metal dummy structures 41 to achieve reinforcement. Structure 41 is patterned in dielectric layer 43, which may be a stack of a mechanically weak HSQ layer 43a and an oxide layer 43b. The bond pad may be connected by vias 42 with the metal dummy structure. In this case, the vias 42 traverse the dielectric layer 44, which may be a stack of silicon nitride, oxide (FSG, USG, PSG oxides, or polymeric), and silicon nitride (or oxy-nitride) layers. Vias 42 do not have to be located at the periphery of bond pad 40.

(26) As another embodiment of the invention, FIG. 5 shows a simplified top view of a bond pad 50 overlying a multi-level reinforcing hierarchy of layers with circuit portions 51 and dummy structures 52. Using identical reference numerals for the same entities, FIG. 6 illustrates a schematic and simplified cross section through the reinforcing hierarchy of layers. The dummy structures are laid out on two complete levels, while the circuit portion consumes part of the bond pad area on another level. As an example, the circuit portion may constitute part of a protection device against electrostatic discharge, especially its interconnection and resistor parts. Another example are interconnective and resistive portions of the circuit. The circuit portion may optionally be connected by via 53 to moat 54 diffused into the silicon substrate 55.

Claims , **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Huan et al. (U.S. Patent Application Publication # 2003/0020163 A1).

1. Huang et al. (figures 1 to 2D) specifically figure 2A-2C show a semiconductor device, comprising: bonding pads **228** that are formed on a semiconductor substrate **200**; an upper copper layer **214** that is formed on the lower surface of said bonding pads with a barrier metal interposed; and a lower copper layer **202** that is formed closer to said semiconductor substrate than said upper copper layer; wherein a copper area of said lower

copper layer under said bonding pads is equal to or lower than that of said upper copper layer.

2. A semiconductor device according to claim 1, Huang et al. show wherein said lower copper layer is electrically insulated from said upper copper layer.

3. A semiconductor device according to claim 1, Huang et al. show wherein the copper area ratio of said upper copper layer is greater than that of other copper layers that are formed as circuit interconnects on said semiconductor substrate.

4. A semiconductor device according to claim 1, Huang et al. show wherein the copper area ratio of said upper copper layer is at least 70%.

5. A semiconductor device according to claim 1, Huang et al. show wherein the planar dimensions of said bonding pads and said upper copper layer are substantially equal.

6. A semiconductor device according to claim 1, Huang et al. show wherein said upper copper layer is constituted by a plurality of copper layers.

7. A semiconductor device according to claim 6, Huang et al. show wherein the copper area ratios of each copper layer of said upper copper layer are substantially the same.

8. A semiconductor device according to claim 6, Huang et al. further comprising: interlevel dielectric films that are

provided between each of the copper layers of said upper copper layer; and via-plugs composed of copper that are embedded in said interlevel dielectric films wherein each of the copper layers of said upper copper layer are connected by way of said via-plugs.

9. A semiconductor device according to claim 8, Huang et al. show wherein the copper layer pattern of the copper layer that is positioned uppermost in said upper copper layer and said via--plugs that are connected to the copper layer pattern are embedded in a dielectric film that is composed of a first material.

10. A semiconductor device according to claim 1, Huang et al. show wherein the copper area ratio of said lower copper layer is at least 15% and not greater than 95%.

11. A semiconductor device according to claim 1, Huang et al. show wherein said lower copper layer is constituted by a plurality of copper layers.

14. A semiconductor device according to claim 13, Huang et al. show wherein each of the copper layers of said lower copper layer are constituted by a copper pattern that is embedded in a dielectric film that is composed of a second material having a lower relative dielectric constant than said first material.

42. Huang et al. (figures 1 to 2D) specifically figure 2A-2C show a semiconductor device comprising: a bonding region in which a bonding pad **228** is formed; an internal circuit region provided inside of said

bonding region, said internal circuit region having a multilevel wiring structure that includes a plurality of copper interconnect layers **214,308** at a first level and a plurality of copper interconnect layers **202,208** at second level; and

a copper layer formed in said bonding region under said bonding pad in electrical contact therewith, one of said copper interconnect layers at said first level being elongated from said internal circuit region to said bonding region under said copper layer in electrical isolation therefrom.

43. The device as claimed in claim 42, Huang et al. show wherein one of said copper interconnect layers at said second level is further elongated from said internal circuit region to said bonding region under said copper layer in electrical isolation from said copper layer and from one of said copper interconnect layers at said first level.

44. The device as claimed in claim 42, Huang et al. show wherein said copper layer includes first and second copper layers and a via-plug sandwiched therebetween.

45. The device as claimed in claim 44, Huang et al. show wherein said multilevel wiring structure further includes a plurality of copper interconnect layers at a third level and a plurality of copper interconnect layers at a fourth level, said first copper layer being formed at said third level and said second copper layer being formed at said fourth level.

46. The device as claimed in claim 45, Huang et al. show wherein said bonding pad is in electrical contact with said second copper

layer, and one of said copper interconnect layers at said fourth level has an electrical contact with said second copper layer.

[0029] Referring to FIG. 2A, a bonding pad structure having a dielectric layer 226 thereon is shown. The bonding pad structure comprises a substrate 200, conductive layers 202, 208 and 214, conductive plugs 207a-207e and 213a-213e, dielectric layers 204, 206, 210, 212 and 216, and a dielectric layer 226. The substrate 200 comprises a semiconductor wafer comprising a plurality of IC device regions therein which are not shown for simplicity, and the semiconductor wafer preferably comprises, but is not limited to: a silicon wafer. The semiconductor wafer can also comprise dielectric materials such as silicon dioxide and diamond-like carbon as well as germanium, gallium arsenide and indium arsenide. The Conductive layers 202, 208 and 214 preferably comprise, but are not limited to: coppers layers and copper alloy layers. The conductive layers 202, 208 and 214 can also be aluminum layers and aluminum alloy layers. More particularly, the method used to form the conductive layers 202, 208 and 214 comprises, but is not limited to: a dual damascene process. The conductive layers 202, 208 and 214 can also be formed by using physical vapor deposition, chemical vapor deposition, electro-chemical deposition and chemical mechanical polishing. The thicknesses of the conductive layers 202, 208 and 214 are from about 2500 angstrom to about 8000 angstrom. The conductive plugs 207a-207e and 213a-213e are preferably, but are not limited to: copper plugs and copper alloy plugs. Other conductive materials such as aluminum, aluminum alloys and tungsten can also be used. The conductive plugs 207a-207e and 213a-213e can be formed by using conventional techniques such as dry etching, wet etching, physical vapor deposition, chemical vapor deposition and dual damascene process. The dielectric layers 204, 206, 210, 212 and 216 preferably comprise, but are not limited to: low-k dielectric layers such as a silk layer, a fluorosilicate glass (FSG) layer, a hydrogen silsesquioxane (HSQ) layer and a methyl silsesquioxane (MSQ) layer. Other dielectric materials such as silicon dioxide and silicon nitride can also be used. The dielectric layers 204, 206, 210, 212 and 216 can be formed by using any conventional technique such as physical vapor deposition, chemical vapor deposition and chemical mechanical polishing. The dielectric layers 204, 206, 210, 212 and 216 have a thickness of from about 2500 angstrom to about

8000 angstrom. The dielectric layer 226 preferably comprises, but is not limited to: a silicon dioxide layer. A silicon nitride layer and a combination layer of silicon dioxide and silicon nitride can also be used. The method used to form the dielectric layer 226 preferably comprises, but is not limited to: by a plasma enhanced chemical vapor deposition. Other conventional deposition method such as physical vapor deposition and chemical vapor deposition can be used. The dielectric layer 226 has a thickness of from about 10000 angstrom to about 25000 angstrom.

[0030] Referring to FIG. 2B, the dielectric layer 226 is etched to form holes or trenches and expose the conductive layer 214, and a conductive layer 228 and via plugs 224a and 224b are formed. A barrier layer comprising a Ti/TiN layer and a Ta/TaN layer is formed previous to the formation of the conductive layer 228, but it is omitted for simplicity here. The dielectric layer 226 is etched preferably by a dry etching process, but other etching methods such as wet etching should not be excluded. The dimension of the holes or trenches is from about 2 micron to about 8 micron, and is preferably about 5 micron. The conductive layer 228 preferably comprises, but is not limited to: an aluminum layer and an aluminum alloy layer. Other conductive materials met the requirements of this invention should not be excluded. The via plugs 224a and 224b are preferably formed together with the conductive layer 228. The method used to form the conductive layer 228 and the via plugs 224a and 224b comprise, but is not limited to: physical vapor deposition. More particularly, instead of conformal growth over a large opening, the conductive layer 228 and the via plugs 224a and 224b are preferably formed by using a gap fill process. With proper process control, the "bird' beak" shown in FIG. 1B and FIG. 1C will not appear thereby prevents the cracks possibly formed at the corners shown in FIG. 1D. The thickness of the conductive layer 228 is from about 10000 angstrom to about 15000 angstrom.

[0031] Referring to FIG. 2C, the conductive layer 228 is etched to expose the dielectric layer 226 and form the bonding pad 228, and a passivation layer 230 is formed thereon and etched to form a pad window 232. Furthermore, a controlled collapse chip connection (C4) pad or bump structure 234 is formed to connect the bonding pad 228. The method used to etch the conductive layer 228 comprises dry etching and wet etching, and it is preferably a dry etching method. The top view of the

bonding pad 228 is shown in FIG. 2D. The passivation layer 230 comprises a silicon dioxide layer, a silicon nitride layer, a SiO.sub.2 and Si.sub.3N.sub.4 layer, a Si.sub.3N.sub.4, SiO.sub.2 and Si.sub.3N.sub.4 layer and a SiO.sub.2, Si.sub.3N.sub.4 and SiO.sub.2 layer. The passivation layer 230 can be formed by using conventional methods such as chemical vapor deposition and physical vapor deposition, and it is preferably a plasma enhanced chemical vapor deposition process. The thickness of the passivation layer 230 is from about 10000 angstrom to about 15000 angstrom. The pad window 232 is formed by using conventional methods such as photolithography, dry etching and wet etching. The contour of the pad window 232 comprises, but it is not limited to: a circle. Other geometrical contours without any sharp corner should not be excluded. The diameter of the pad window 232 is about 40 micron to about 90 micron. The plated C4 pad or bump structure 234 connects directly to the bonding pad 228 through the pad window 232. The bump structure 234 comprises Pb--Sn solder and is provided on integrated circuit chips for making interconnections to substrates.

[0032] The invention modifies the pad structure above the top copper layer 114 as shown in FIG. 1B and FIG. 1C which has a square pad window in the passivation layer 118, a sizing-up aluminum pad 120 to a new one having a dielectric layer 226 having the via plugs 224a and 224b connecting the top conductive layer 214 and the bonding pad 228, the bonding pad 228 and a pad window 232 having a contour without any sharp corner in the passivation layer 230 as shown in FIG. 2C. The advantages of this pad structure include: first, during tests such as probing, as the probe penetrates the bonding pad 228 or renders the bonding pad 228 peeling, the dielectric layer 226 can prevent the conductive layer 214 from exposing to the atmospheric conditions. Second, the dielectric layer 226 serving as a buffer layer can effectively degrade the bonding force directly coupling to the underlying pad structure and prevent cracks and peeling during packaging or testing. Third, instead of conformal growth, the bonding pad 228 is formed by gap fill, cracks at sharp corners will not occur. Fourth, because the via plugs connecting the top conductive layer 214 and the bonding pad 228 are uniformly distributed along the contour of the pad window 232, the shear force of packaging or testing will be distributed and dispersed and cracks can be avoided. Fifth, because the dielectric layer 226

is formed over the whole integrated circuit, it can clamp the underlying pad structure and prevent the underlying pad structure from peeling.

The listed references are cited as of interest to this application, but not applied at time.

Field of Search	Date
U.S. Class and subclass: 257/700,701,758,459,784,774,680,756,750,734	9/30/05
Other Documentation: foreign patents and literature in 257//700,701,758,459,784,774,680,756,750,734	9/30/05
Electronic data base(s): U.S. Patents EAST	9/30/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
9/30/05